



	IN THE UNI	TED STATES PAT	ENT AND TRADEMARK OFFICE
In re a	application of:	Miura et al.	
Serial	No.:	10/078,766	
Filed:	:	February 19, 2002	
For:		PROCESS FOR EI	LECTROPLATING SILICON WAFERS
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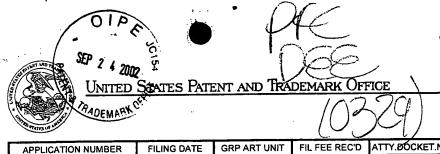
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Correct data Error in 1. [X] Applicant's name and address 1. Takeshi MIURA 2. [] Applicant's address 2. 3. 3. [] Title 4. [] Filing Date 4. 5. [] Serial Number 5. 6. [] Foreign/PCT Application Re: 6. 7. [] Other 7. (complete the following applicable item) 3. A. [] The correction(s) is/are not due to any error by applicant and no fee is due. OR B. [X] At least one of the above corrections is due to applicant's error and the fee therefor, under 37 C.F.R. 1.19(h), of \$25.00 is paid as follows: [] Enclosed is check for \$25.00. [X] Charge Account 04-1105 the sum of \$25.00. SIGNATURE OF PRACTITIONER Peter F. Corless Reg. No. 33,860 (type or print name of practitioner) **EDWARDS & ANGELL, LLP** Dike, Bronstein, Roberts & Cushman, IP Group P.O. Box 9169 Tel. No. (617) 523-3400

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DRAWINGS TOT CLAIMS IND CLAIMS

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Applicant(s)

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Assignment For Published Patent Application

Shipley Company, L.L.C., Malborough, MA;

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Foreign Applications

If Required, Foreign Filing License Granted 04/02/2002

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Non-Publication Request: No

Early Publication Request: No

Title

Process for electroplating silicon wafers

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